

This listing of claims will replace all prior versions, and listings of claims in the application:

Amendments to the Claims:

Please cancel claims 1-24 without prejudice and new claims 25-52.

1. - 24. (Cancelled)

25. (New) A method of programming a laser programmable integrated circuit,
comprising:

providing an alignment structure on the integrated circuit, the alignment structure
formed using a planarized process, the alignment structure comprising a substrate, a first region
formed on the substrate, and a second region formed on the substrate adjacent to the first region,
the first region characterized by a first optical reflectiveness value and the second region
characterized by a second optical reflectiveness value different from the first optical
reflectiveness value;

aligning the integrated circuit using the alignment structure;
referencing a first programmable element located on the integrated circuit using a
laser; and

programming the first programmable element using the laser.

26. (New) The method of claim 25 wherein the integrated circuit is a
programmable logic device (PLD) comprising a plurality of logical elements and a plurality of
interconnections between the logical elements.

27. (New) The method of claim 26 wherein programming the first
programmable element using the laser comprises configuring a logical element from the plurality
of logical elements using the laser.

28. (New) The method of claim 26 wherein programming the first
programmable element using the laser comprises configuring an interconnection from the
plurality of interconnections using the laser.

1 29. (New) The method of claim 25 wherein the programmable element is a
2 fuse, an antifuse, an EPROM, a flash, an EEPROM, or a SRAM cell.

1 30. (New) The method of claim 25 further comprising:
2 programming a second programmable element located on the integrated circuit
3 using in-system programming.

1 31. (New) The method of claim 25 wherein the second region of the alignment
2 structure comprises:

3 a first conductive layer;
4 a second conductive layer formed above the first conductive layer,
5 an first insulating layer, between the first and second conductive layers, wherein
6 the first insulating layer has a first opening for electrically coupling the first and second
7 conductive layers; and
8 a plug layer filling the first opening, wherein the first plug layer has a cored
9 region, whereby a topographical roughness formed by the cored region scatters incident
10 radiation.

1 32. (New) The method of claim 31 wherein the second region of the alignment
2 structure further comprises:

3 a third conductive layer formed above the second conductive layer; and
4 a second insulating layer, between the second and third conductive layers,
5 wherein the second conductive layer has a second opening, stacked above the first opening, for
6 electrically coupling the third and second conductive layers, whereby the second opening
7 aggravates the topographical roughness formed by the cored region.

1 33. (New) The method of claim 25 wherein the second region of the alignment
2 structure comprises:

3 a contact opening formed on the substrate; and

4 a first plug layer filling the contact opening, the first plug layer having a first
5 depressed region in the contact opening, whereby a topographical roughness formed by the first
6 depressed region scatters incident radiation.

1 34. (New) The method of claim 33 wherein the second region of the alignment
2 structure further comprises:

3 a first via opening stacked on top of the contact opening, whereby the first via
4 opening enhances the topographical roughness formed by the first depressed region.

1 35. (New) The method of claim 34 wherein the second region of the alignment
2 structure further comprises:

3 a second via opening stacked on top of the first via opening and second via
4 opening, whereby the second via opening further enhances the topographical roughness.

1 36. (New) The method of claim 25 wherein:

2 the first region comprises a first portion and a second portion, wherein the first
3 portion of the first region is perpendicular to the second portion of the first region; and

4 the second region comprises a first portion and a second portion, wherein the first
5 portion of the second region is adjacent to the first portion of the first region, and the second
6 portion of the second region is adjacent to the second portion of the first region.

1 37. (New) A method of programming a laser programmable integrated circuit,
2 comprising:

3 providing an alignment structure on the integrated circuit, the alignment structure
4 formed in a planarized semiconductor process, the alignment structure comprising:

5 a substrate;

6 a first region formed on the substrate, the first region characterized by a
7 first optical reflectiveness value; and

8 a second region formed on the substrate adjacent to the first region, the
9 second region characterized by a second optical reflectiveness value different from the first
10 optical reflectiveness value, the second region comprising:
11 a first conductive layer;
12 a second conductive layer;
13 an first insulating layer, between the first and second conductive
14 layers, wherein the first insulating layer has a first opening for electrically coupling the first and
15 second conductive layers; and
16 a plug layer filling the first opening, wherein the first plug layer
17 has a cored region, whereby a topographical roughness formed by the cored region scatters
18 incident radiation.;
19 aligning the integrated circuit using the alignment structure;
20 referencing a first programmable element located on the integrated circuit using a
21 laser; and
22 programming the first programmable element using the laser.

1 38. (New) A method of programming a programmable logic integrated circuit
2 comprising:
3 aligning the programmable logic integrated circuit, fabricated using a planarized
4 process, using a laser to scan a plurality of alignment structures formed on the integrated circuit,
5 wherein each alignment structure in the plurality of alignment structures comprises:
6 a first region formed on a substrate of the integrated circuit, the first region
7 characterized by a first optical reflectiveness value; and
8 a second region formed on the substrate adjacent to the first region, the
9 second region characterized by a second optical reflectiveness value different from the first
10 optical reflectiveness value; and
11 programming a first programmable element of the programmable logic integrated
12 circuit using the laser.

1 39. (New) The method of claim 38 wherein the first programmable element is
2 a fuse.

1 40. (New) The method of claim 38 wherein the second region of each
2 alignment structure comprises:
3 a first conductive layer;
4 a second conductive layer formed above the first conductive layer,
5 an first insulating layer, between the first and second conductive layers, wherein
6 the first insulating layer has a first opening for electrically coupling the first and second
7 conductive layers; and
8 a plug layer filling the first opening, wherein the first plug layer has a cored
9 region, whereby a topographical roughness formed by the cored region scatters incident
10 radiation.

1 41. (New) The method of claim 40 wherein the second region of each
2 alignment structure further comprises:
3 a third conductive layer formed above the second conductive layer; and
4 a second insulating layer, between the second and third conductive layers,
5 wherein the second conductive layer has a second opening, stacked above the first opening, for
6 electrically coupling the third and second conductive layers, whereby the second opening
7 aggravates the topographical roughness formed by the cored region.

1 42. (New) The method of claim 38 wherein the second region of each
2 alignment structure comprises:
3 a contact opening formed on the substrate; and
4 a first plug layer filling the contact opening, the first plug layer having a first
5 depressed region in the contact opening, whereby a topographical roughness formed by the first
6 depressed region scatters incident radiation.

1 43. (New) The method of claim 42 wherein the second region of the alignment
2 structure further comprises:
3 a first via opening stacked on top of the contact opening, whereby the first via
4 opening enhances the topographical roughness formed by the first depressed region.

1 44. (New) The method of claim 43 wherein the second region of the alignment
2 structure further comprises:
3 a second via opening stacked on top of the first via opening and second via
4 opening, whereby the second via opening further enhances the topographical roughness.

1 45. (New) The method of claim 38 wherein aligning the programmable logic
2 integrated circuit comprises:
3 detecting a position of a first alignment structure from the plurality of alignment
4 structures using the laser;
5 detecting a position of a second alignment structure from the plurality of
6 alignment structures using the laser; and
7 aligning the programmable logic integrated circuit using the first alignment
8 structure and the second alignment structure.

1 46. (New) The method of claim 45 wherein detecting the position of the first
2 alignment structure using the laser comprises:
3 scanning the first alignment structure using the laser along a line traversing the
4 first region and the second region of the first alignment structure;
5 detecting a change in reflectivity as the laser scans across the first region and the
6 second region; and
7 determining the position of the first alignment structure based upon the change in
8 reflectivity.

1 47. (New) The method of claim 38 wherein:

2 the first region comprises a first portion and a second portion, wherein the first
3 portion of the first region is perpendicular to the second portion of the first region; and

4 the second region comprises a first portion and a second portion, wherein the first
5 portion of the second region is adjacent to the first portion of the first region, and the second
6 portion of the second region is adjacent to the second portion of the first region.

1 48. (New) The method of claim 38 wherein each alignment structure from the
2 plurality of alignment structures has a first portion extending in a first direction and a second
3 portion extending in a second direction transverse to the first direction.

1 49. (New) The method of claim 38 wherein the first programmable element is
2 used to configure functionality of programmable logic of the integrated circuit.

1 50. (New) The method of claim 38 wherein the plurality of alignment
2 structures comprises at least three alignment structures.

1 51. (New) The method of claim 38 wherein the first programmable element is
2 used to implement a redundancy scheme of the integrated circuit.

1 52. (New) The method of claim 38 wherein aligning the programmable logic
2 integrated circuit comprises:

3 scanning a first alignment structure from the plurality of alignment structures in a
4 first direction and in a second direction transverse to the first direction.